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Assertion-Based and Constrained Random Verification of AHB Protocol Using UVM

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Abstract: The Advanced High-performance Bus (AHB) protocol, defined under the ARM AMBA specification, is widely adopted in System-on-Chip (SoC) designs for high-speed communication between processors, memory controllers, and peripheral devices. Ensuring functional correctness and protocol compliance of AHB-based designs is critical due to increasing system complexity and stringent performance requirements. This paper presents the design and comprehensive verification of the AHB protocol using the Universal Verification Methodology (UVM) framework in SystemVerilog. The proposed verification environment is structured with reusable and scalable UVM components including drivers, monitors, sequencers, agents, scoreboards, and coverage collectors. AHB master and slave models are developed to validate transaction types such as single transfer, burst transfer, pipelined operations, and response handling mechanisms. Functional coverage metrics and constrained-random stimulus generation are employed to achieve exhaustive verification of address, data, and control signal interactions. Assertions are integrated to monitor protocol timing and handshaking requirements, ensuring compliance with AMBA specifications. Simulation results demonstrate effective bug detection, improved coverage closure, and enhanced verification efficiency compared to traditional directed testing approaches. The study highlights the advantages of UVM-based verification in achieving modularity, reusability, and scalability for complex bus protocol validation, making it suitable for modern SoC verification environments.

Keywords: Advanced High-performance Bus (AHB); AMBA Protocol; Universal Verification Methodology (UVM); SystemVerilog; Functional Verification.

I. INTRODUCTION

The rapid growth of System-on-Chip (SoC) complexity has significantly increased the need for robust and scalable verification methodologies capable of ensuring functional correctness and protocol compliance. Modern SoCs integrate multiple IP cores communicating through standardized on-chip bus architectures, among which the Advanced High-Performance Bus (AHB), defined under the ARM AMBA specification, plays a crucial role in high-speed data transfer between processors, memory controllers, and peripherals. As transaction-level concurrency, pipelining, burst transfers, and split responses increase protocol complexity, traditional directed testing approaches become insufficient to guarantee exhaustive verification coverage.

Universal Verification Methodology (UVM), built upon SystemVerilog, has emerged as an industry-standard framework for functional verification due to its modularity, reusability, and scalability. Additionally, assertion-based verification (ABV) and constrained random verification (CRV) techniques have proven highly effective in detecting corner-case protocol violations and achieving functional coverage closure. This research focuses on the design and implementation of a UVM-based verification environment incorporating SystemVerilog assertions and constrained random stimulus generation to validate the AHB protocol. The study demonstrates how combining ABV and CRV enhances protocol compliance checking, improves bug detection efficiency, and ensures reliable SoC integration.

II. OBJECTIVES

The primary objective of this research is to develop and validate a comprehensive verification framework for the AHB protocol using UVM integrated with assertion-based and constrained random verification techniques. The specific objectives include:

- Designing a reusable UVM-based testbench architecture for AHB master-slave communication.
- Implementing constrained random stimulus to generate diverse transaction scenarios including single, burst, and pipelined transfers.
- Developing System Verilog assertions to monitor protocol timing, handshaking, and signal transitions.
- Measuring functional coverage to ensure verification

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completeness.

- Evaluating verification efficiency in terms of bug detection capability and coverage closure.

III. LITERATURE REVIEW

Verification methodologies have evolved significantly over the past decades. Bergeron (2003) introduced reusable verification components and transaction-level modeling concepts that later influenced UVM development. Spear (2012) emphasized constrained random stimulus generation as a powerful technique for exploring corner cases in complex digital systems.

ARM's AMBA specification (ARM Ltd., 2010) provides the formal definition of AHB protocol timing, burst types, arbitration, and response handling, serving as the foundational reference for protocol verification. Love (2010) and other system-level studies have highlighted the importance of bus-level synchronization in high-performance computing systems.

Research by Bhasker (2004) demonstrated the advantages of SystemVerilog assertions for detecting protocol timing violations during simulation. Jain et al. (2016) explored UVM-based verification of bus architectures and reported improved coverage metrics compared to traditional Verilog testbenches.

Recent studies emphasize coverage-driven verification strategies. Foster (2004) introduced assertion-based verification frameworks that significantly reduce debugging time. Kumar and Mishra (2018) demonstrated constrained random verification for AMBA protocols, showing improved functional coverage and reduced verification cycles. These studies collectively establish that integrating ABV and CRV within a UVM framework provides a scalable and systematic solution for verifying complex communication protocols such as AHB.

IV. PROPOSED METHODOLOGY

The proposed methodology involves constructing a layered UVM testbench environment to verify AHB protocol compliance. The Device Under Test (DUT) consists of an AHB master and slave interface model implementing address, data, and control signal interactions according to AMBA specifications.

The integration of scoreboards enabled real-time comparison of expected and actual transaction outputs, ensuring data integrity verification. The overall verification strategy achieved faster coverage closure and improved confidence in AHB protocol compliance.

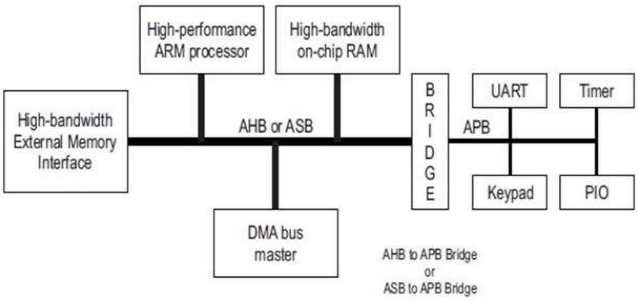

Figure 1: AMBA bus Block Diagram

The UVM testbench includes key components such as sequencer, driver, monitor, agent, scoreboard, and coverage collector. Constrained random sequences are developed to generate randomized address phases, burst lengths, and response conditions. Functional coverage groups are defined to monitor transaction types, burst modes (INCR, WRAP), transfer sizes, and response types (OKAY, ERROR, RETRY, SPLIT).

SystemVerilog assertions are embedded to monitor protocol rules including HREADY handshaking, address alignment, burst termination, and response timing constraints. Assertions operate concurrently during simulation, immediately flagging protocol violations.

V. VERIFICATION METHODOLOGY

The verification environment follows a coverage-driven verification (CDV) approach. The UVM testbench architecture is organized into reusable components enabling scalability for future protocol extensions.

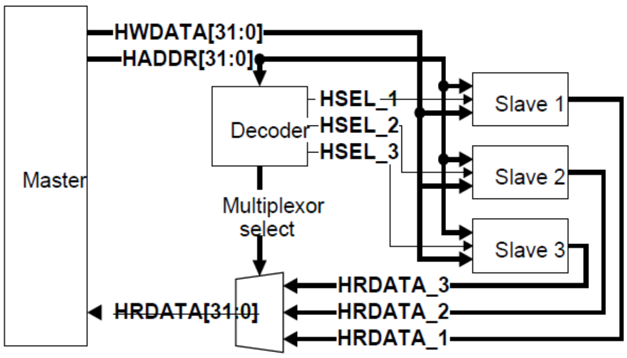

Figure 2: AHB block diagram

Constrained random verification is implemented using

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randomized sequence items with defined constraints to ensure legal and boundary-value transactions. This approach enables automatic exploration of corner cases without manually writing directed tests.

Assertion-based verification complements CRV by enforcing protocol compliance at runtime. Immediate and concurrent assertions are used to check signal stability, setup and hold conditions, burst sequencing, and state transitions.

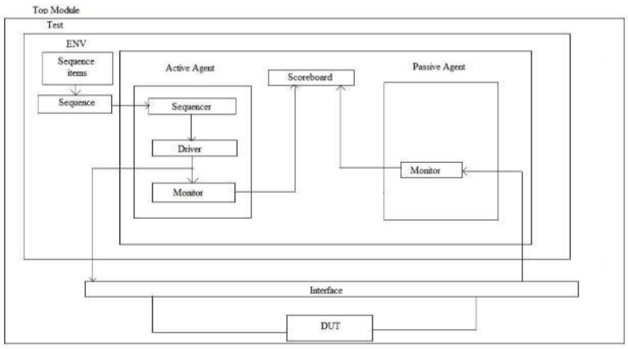

Figure 3: Universal Verification Methodology (UVM)

Coverage metrics include functional coverage, code coverage, and assertion coverage. The verification process continues iteratively until coverage closure is achieved, ensuring comprehensive validation of protocol behavior.

VI. RESULTS AND EVALUATION

Simulation results were obtained using a SystemVerilog-compatible simulator supporting UVM libraries. Constrained random sequences successfully generated diverse transaction scenarios including single transfers, incrementing bursts, and wrapping bursts. Functional coverage exceeded 95%, demonstrating extensive exploration of protocol states.

Assertions effectively detected timing violations and incorrect handshaking conditions introduced during fault injection testing. Compared to directed testing, the UVM-based constrained random environment reduced verification effort and improved bug detection efficiency.

The integration of scoreboards enabled real-time comparison of expected and actual transaction outputs, ensuring data integrity verification. The overall verification strategy achieved faster coverage closure and improved confidence in AHB protocol compliance.

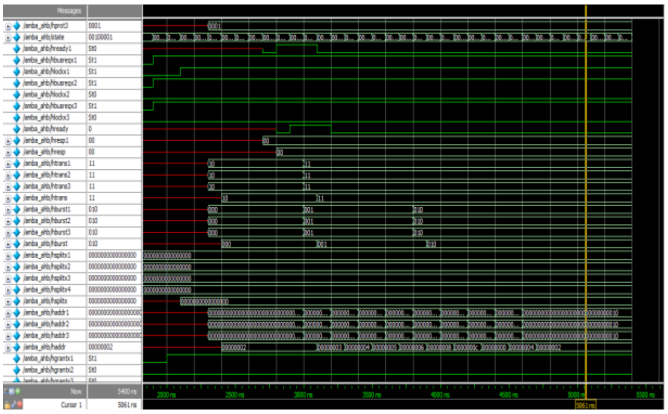

Figure 4: Simulation result of AHB protocol

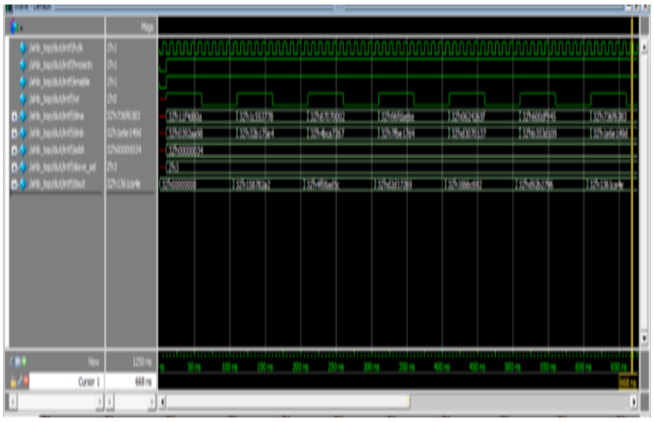

Figure 5: UVM testbench environment

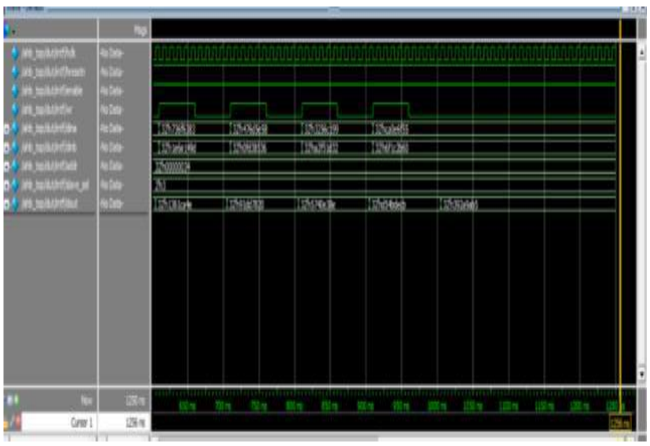

Figure 6: Extension of UVM testbench environment

VII. CONCLUSION

This research presented an assertion-based and constrained random verification framework for the AHB protocol using UVM methodology. The proposed approach integrates reusable

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UVM components, functional coverage models, and SystemVerilog assertions to achieve comprehensive protocol validation. Results demonstrate improved verification efficiency, enhanced corner-case detection, and effective coverage-driven testing compared to traditional approaches. The methodology provides a scalable and industry-relevant solution for SoC bus protocol verification. Future work may include formal verification integration and extension to advanced AMBA protocols such as AXI.

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