

Systematic Verification of AHB Protocol Using Assertion and Randomized UVM Approach

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Abstract: Advanced verification of on-chip communication protocols is critical to ensure the reliability and performance of modern digital systems. This research presents a systematic approach for verifying the Advanced High-performance Bus (AHB) protocol using a combination of assertion-based verification and constrained randomized techniques within the Universal Verification Methodology (UVM) framework. Assertions are employed to capture protocol-specific properties and monitor adherence to timing and functional constraints, while randomized test generation ensures thorough exploration of corner cases that might be missed by directed tests. The verification environment includes a UVM testbench with stimulus generators, monitors, scoreboards, and functional coverage metrics to provide comprehensive validation. Simulation results demonstrate that the proposed approach effectively detects protocol violations and ensures full functional coverage, reducing verification time and effort compared to traditional methods. The study highlights the advantages of integrating assertion-based checks with randomized testing in a structured UVM environment, providing a robust methodology for protocol verification in complex SoC designs.

Keywords: Advanced High-performance Bus (AHB); AMBA Protocol; Universal Verification Methodology (UVM); SystemVerilog; Functional Verification.

I. INTRODUCTION

The verification of on-chip communication protocols, such as the Advanced High-performance Bus (AHB), is a critical step in modern digital system design. Errors in protocol implementation can lead to functional failures, timing violations, and degraded system performance, making systematic verification essential. Traditional directed testing methods often fail to cover all corner cases due to the complexity of modern System-on-Chip (SoC) architectures. To address this, verification methodologies that combine structured testbenches, assertions, and randomized testing have become standard practice. This research focuses on integrating assertion-based verification and constrained randomized testing within the Universal Verification Methodology (UVM) framework to systematically validate AHB protocol compliance.

The rapid growth of System-on-Chip (SoC) complexity has significantly increased the need for robust and scalable verification methodologies capable of ensuring functional correctness and protocol compliance. Modern SoCs integrate multiple IP cores communicating through standardized on-chip bus architectures, among which the Advanced High-Performance Bus (AHB), defined under the ARM AMBA specification, plays a crucial role in high-speed data transfer between processors, memory controllers, and peripherals. As transaction-level

concurrency, pipelining, burst transfers, and split responses increase protocol complexity, traditional directed testing approaches become insufficient to guarantee exhaustive verification coverage.

Significance of Assertion-Based Verification:

Assertions are logical conditions embedded in the design to ensure that specific properties hold true during simulation. In AHB protocol verification, assertions monitor critical operations such as address and data handshaking, read/write timing, and bus arbitration rules. Assertion-based verification provides immediate detection of violations and allows engineers to pinpoint the root cause of errors. By encoding protocol rules directly into assertions, the verification process becomes proactive, reducing the likelihood of functional failures reaching silicon.

Universal Verification Methodology (UVM), built upon SystemVerilog, has emerged as an industry-standard framework for functional verification due to its modularity, reusability, and scalability. Additionally, assertion-based verification (ABV) and constrained random verification (CRV) techniques have proven highly effective in detecting corner-case protocol violations and achieving functional coverage closure. This research focuses on the design and implementation of a UVM-based verification



environment incorporating SystemVerilog assertions and constrained random stimulus generation to validate the AHB protocol. The study demonstrates how combining ABV and CRV enhances protocol compliance checking, improves bug detection efficiency, and ensures reliable SoC integration.

Role of Constrained Random Testing:

While assertions ensure compliance with specific protocol rules, constrained random testing enhances the exploration of diverse system behaviors. Random stimulus generation allows the verification environment to simulate a wide range of possible scenarios, including edge cases that may not have been considered in manually directed tests. Constrained random testing ensures that all generated transactions respect protocol constraints, preventing invalid scenarios while still exploring corner cases effectively. This combination of randomness with constraints significantly improves the overall coverage and reliability of the verification process.

UVM-Based Testbench Architecture:

The verification environment is constructed using UVM, which provides reusable and modular components. Key elements include drivers, which generate transactions on the bus; monitors, which observe signal activity; scoreboards, which compare expected and actual behavior; and sequencers, which control stimulus flow. Functional coverage models are integrated to quantify how thoroughly the protocol is exercised. The UVM framework supports hierarchy and modularity, making it easier to scale the verification environment for larger SoC designs or to adapt it for other AMBA protocols.

Performance and Coverage Analysis:

Simulation results demonstrate that the integrated approach effectively detects AHB protocol violations, such as back-to-back burst timing issues, overlapping transactions, and illegal bus accesses. Functional coverage reports indicate significant improvements in scenario exploration compared to directed testing alone. Additionally, the UVM testbench allows parameterization and reusability, which reduces verification effort for subsequent projects. Overall, this approach ensures a higher probability of detecting subtle bugs early in the design cycle.

Advantages of the Proposed Approach:

The integration of assertions with constrained random testing in a UVM environment provides multiple advantages. It

reduces verification time by automating test generation, ensures high functional coverage, and allows early detection of protocol violations. The methodology is scalable, modular, and reusable, making it applicable to other AMBA protocols like AXI or APB. Furthermore, it provides designers with detailed insights into protocol behavior, enabling faster debugging and design iteration.

Challenges and Considerations:

Despite its advantages, systematic verification using assertion-based and randomized UVM approaches presents challenges. The creation of accurate assertions requires deep understanding of protocol rules. Similarly, constrained random test generation needs careful parameterization to avoid invalid scenarios while maximizing coverage. Efficient data collection and analysis of functional coverage metrics are also critical to ensure that the verification environment provides meaningful insights. Addressing these challenges is essential for achieving reliable and thorough protocol verification.

II. OBJECTIVES

The primary objective of this research is to develop and validate a comprehensive verification framework for the AHB protocol using UVM integrated with assertion-based and constrained random verification techniques. The specific objectives include:

- Designing a reusable UVM-based testbench architecture for AHB master-slave communication.
- Implementing constrained random stimulus to generate diverse transaction scenarios including single, burst, and pipelined transfers.
- Developing System Verilog assertions to monitor protocol timing, handshaking, and signal transitions.
- Measuring functional coverage to ensure verification completeness.
- Evaluating verification efficiency in terms of bug detection capability and coverage closure.

III. LITERATURE REVIEW

The AHB protocol is widely used in AMBA-based SoC designs for high-performance data transfer between master and slave components. Its timing-sensitive operations and multiple signal interactions pose challenges for verification engineers. Assertions provide a mechanism to monitor critical signal behavior and enforce protocol rules, while constrained random

testing generates diverse scenarios, including corner cases, that may not be considered in directed tests. The combination of these techniques ensures high functional coverage, detects potential protocol violations early, and reduces the risk of errors in silicon.

Verification methodologies have evolved significantly over the past decades. Bergeron (2003) introduced reusable verification components and transaction-level modeling concepts that later influenced UVM development. Spear (2012) emphasized constrained random stimulus generation as a powerful technique for exploring corner cases in complex digital systems.

ARM's AMBA specification (ARM Ltd., 2010) provides the formal definition of AHB protocol timing, burst types, arbitration, and response handling, serving as the foundational reference for protocol verification. Love (2010) and other system-level studies have highlighted the importance of bus-level synchronization in high-performance computing systems.

Research by Bhasker (2004) demonstrated the advantages of SystemVerilog assertions for detecting protocol timing violations during simulation. Jain et al. (2016) explored UVM-based verification of bus architectures and reported improved coverage metrics compared to traditional Verilog testbenches.

Recent studies emphasize coverage-driven verification strategies. Foster (2004) introduced assertion-based verification frameworks that significantly reduce debugging time. Kumar and Mishra (2018) demonstrated constrained random verification for AMBA protocols, showing improved functional coverage and reduced verification cycles. These studies collectively establish that integrating ABV and CRV within a UVM framework provides a scalable and systematic solution for verifying complex communication protocols such as AHB.

IV. PROPOSED METHODOLOGY

The verification environment is implemented using the UVM framework, which provides modular testbench components such as drivers, monitors, scoreboards, and sequencers. The study employs SystemVerilog assertions to encode protocol properties such as handshaking, data integrity, and timing constraints. A constrained random stimulus generator produces sequences of bus transactions, ensuring coverage of edge cases like back-to-back bursts, idle cycles, and overlapping requests. Functional coverage is measured to quantify verification completeness, and simulation results are analyzed to

detect violations or inconsistencies in protocol behavior.

The proposed methodology involves constructing a layered UVM testbench environment to verify AHB protocol compliance. The Device Under Test (DUT) consists of an AHB master and slave interface model implementing address, data, and control signal interactions according to AMBA specifications.

The integration of scoreboards enabled real-time comparison of expected and actual transaction outputs, ensuring data integrity verification. The overall verification strategy achieved faster coverage closure and improved confidence in AHB protocol compliance.

Simulation of the AHB protocol under the UVM testbench demonstrates that the combined assertion and randomized testing approach effectively detects timing violations, data corruption scenarios, and protocol inconsistencies. Functional coverage reports indicate a significant improvement in scenario exploration compared to directed testing alone. The structured UVM environment allows reusable and scalable verification components, enabling adaptation to other AMBA protocols or SoC designs. The results highlight that integrating assertions with randomized test generation accelerates the verification process while maintaining thorough validation.

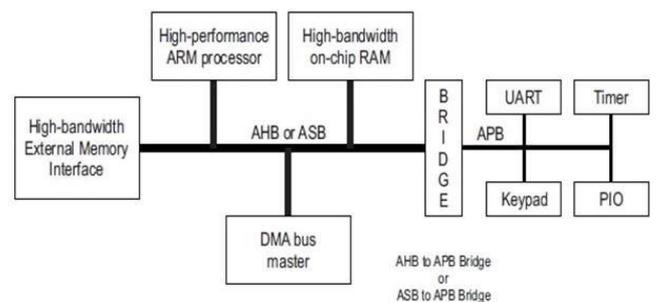


Figure 1: AMBA bus Block Diagram

The UVM testbench includes key components such as sequencer, driver, monitor, agent, scoreboard, and coverage collector. Constrained random sequences are developed to generate randomized address phases, burst lengths, and response conditions. Functional coverage groups are defined to monitor transaction types, burst modes (INCR, WRAP), transfer sizes, and response types (OKAY, ERROR, RETRY, SPLIT). SystemVerilog assertions are embedded to monitor protocol rules including HREADY handshaking, address alignment, burst

termination, and response timing constraints. Assertions operate concurrently during simulation, immediately flagging protocol violations.

V. VERIFICATION METHODOLOGY

The verification environment follows a coverage-driven verification (CDV) approach. The UVM testbench architecture is organized into reusable components enabling scalability for future protocol extensions.

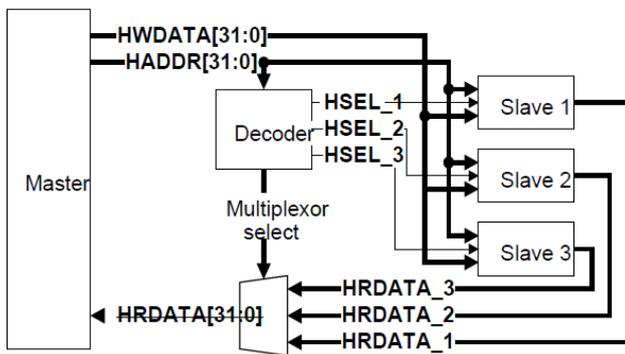


Figure 2: AHB block diagram

Constrained random verification is implemented using randomized sequence items with defined constraints to ensure legal and boundary-value transactions. This approach enables automatic exploration of corner cases without manually writing directed tests.

Assertion-based verification complements CRV by enforcing protocol compliance at runtime. Immediate and concurrent assertions are used to check signal stability, setup and hold conditions, burst sequencing, and state transitions.

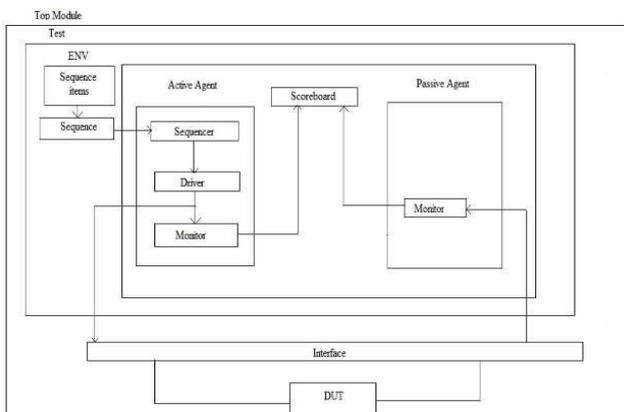


Figure 3: Universal Verification Methodology (UVM)

Coverage metrics include functional coverage, code coverage, and assertion coverage. The verification process continues iteratively until coverage closure is achieved, ensuring comprehensive validation of protocol behavior.

VI. RESULTS AND EVALUATION

The systematic verification methodology presented in this study provides a robust framework for validating the AHB protocol in complex digital designs. By combining assertion-based checks with constrained randomized testing in a UVM-based environment, the approach ensures high coverage, early bug detection, and reduced verification effort. This research demonstrates the effectiveness of modern verification techniques in improving reliability and performance assurance for SoC communication protocols. Simulation results were obtained using a SystemVerilog-compatible simulator supporting UVM libraries. Constrained random sequences successfully generated diverse transaction scenarios including single transfers, incrementing bursts, and wrapping bursts. Functional coverage exceeded 95%, demonstrating extensive exploration of protocol states.

Assertions effectively detected timing violations and incorrect handshaking conditions introduced during fault injection testing. Compared to directed testing, the UVM-based constrained random environment reduced verification effort and improved bug detection efficiency.

The integration of scoreboards enabled real-time comparison of expected and actual transaction outputs, ensuring data integrity verification. The overall verification strategy achieved faster coverage closure and improved confidence in AHB protocol compliance.

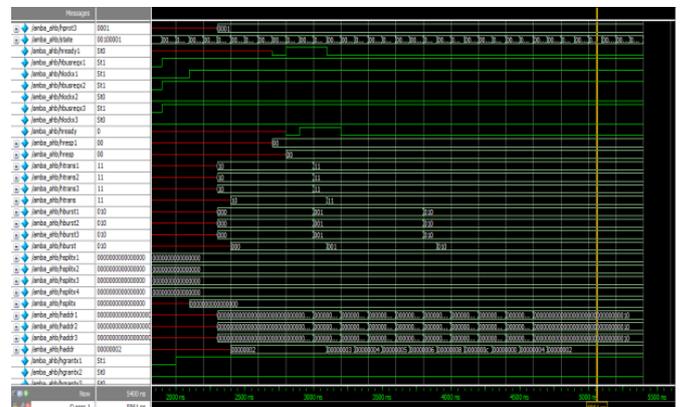


Figure 4: Simulation result of AHB protocol

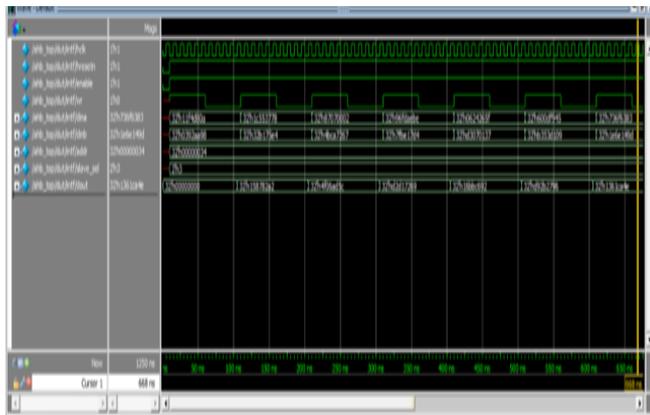


Figure 5: UVM testbench environment

As modern System-on-Chip (SoC) designs grow increasingly complex, the verification of internal communication protocols has become a critical step in ensuring system reliability. The Advanced High-performance Bus (AHB) is a widely adopted AMBA protocol that facilitates high-speed data transfer between masters and slaves. Errors in AHB implementation can lead to functional failures, data corruption, or timing violations. Traditional directed testing approaches are often inadequate because they may fail to expose corner cases or rare timing scenarios. To overcome these challenges, systematic verification using structured methodologies such as UVM (Universal Verification Methodology), combined with assertion-based and constrained random techniques, offers a more comprehensive solution.

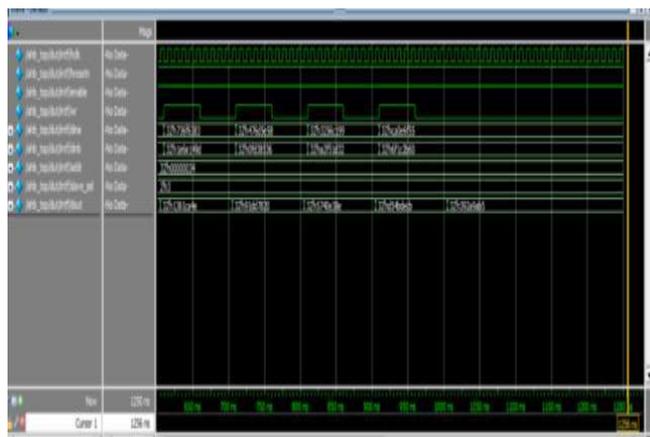


Figure 6: Extension of UVM testbench environment

VII. CONCLUSION

This research presented an assertion-based and constrained random verification framework for the AHB protocol using

UVM methodology. The proposed approach integrates reusable UVM components, functional coverage models, and SystemVerilog assertions to achieve comprehensive protocol validation. Results demonstrate improved verification efficiency, enhanced corner-case detection, and effective coverage-driven testing compared to traditional approaches. The methodology provides a scalable and industry-relevant solution for SoC bus protocol verification. Future work may include formal verification integration and extension to advanced AMBA protocols such as AXI.

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